(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 392 895 B1**

(12) # EUROPEAN PATENT SPECIFICATION

(45) Date of publication of patent specification : **13.12.95 Bulletin 95/50**

(51) Int. Cl.[6] : **G11C 16/06**

(21) Application number : **90400885.1**

(22) Date of filing : **30.03.90**

(54) **Flash EEprom system**

Divisional application 94105842.2 filed on 30/03/90.

(30) Priority : **13.04.89 US 337566**

(43) Date of publication of application : **17.10.90 Bulletin 90/42**

(45) Publication of the grant of the patent : **13.12.95 Bulletin 95/50**

(84) Designated Contracting States : **DE FR GB**

(56) References cited :
COMPUTER DESIGN, vol. 28, no. 5, 1st March 1989, pages 30,32, Tulsa, OK, US; R. WILSON: "1-Mbit flash memories seek their role in system design"

(73) Proprietor : **SUNDISK CORPORATION**
4401 Great America Parkway,
Suite 150
Santa Clara, California 95054 (US)

(72) Inventor : **Harari, Eliyahou**
104 Auzerais Court
Los Gatos, California 95054 (US)
Inventor : **Norman, Robert D.**
6656 Pebblewood Court
San Jose, California 95120 (US)
Inventor : **Mehrotra, Sanjay**
735 Berkshire Place
Milpitas, California 95035 (US)

(74) Representative : **Kopacz, William James**
83, Avenue Foch
F-75116 Paris (FR)

EP 0 392 895 B1

Description

Background of the Invention

This invention relates generally to semiconductor electrically erasable programmable read only memories (EEprom), and specifically to a system of integrated circuit Flash EEprom chips.

Computer systems typically use magnetic disk drives for mass storage of data. However, disk drives are disadvantageous in that they are bulky and in their requirement for high precision moving mechanical parts. Consequently they are not rugged and are prone to reliability problems, as well as consuming significant amounts of power. Solid state memory devices such as DRAM's and SRAM's do not suffer from these disadvantages. However, they are much more expensive, and require constant power to maintain their memory (volatile). Consequently, they are typically used as temporary storage.

EEprom's and Flash EEprom's are also solid state memory devices. Moreover, they are nonvolatile, and retain their memory even after power is shut down. However, conventional Flash EEprom's have a limited lifetime in terms of the number of write (or program)/erase cycles they can endure. Typically the devices are rendered unreliable after 10^2 to 10^3 write/erase cycles. Traditionally, they are typically used in applications where semi-permanent storage of data or program is required but with a limited need for reprogramming.

Accordingly, it is an object of the present invention to provide a Flash EEprom memory system with enhanced performance and which remains reliable after enduring a large number of write/erase cycles.

It is another object of the present invention to provide an improved Flash EEprom system which can serve as non-volatile memory in a computer system.

It is another object of the present invention to provide an improved Flash EEprom system that can replace magnetic disk storage devices in computer systems.

It is another object of the present invention to provide a Flash EEprom system with improved erase operation.

Summary of the Invention

These and additional objects are accomplished by improvements in the architecture of a system of EEprom chips, and the circuits and techniques therein.

According to the present invention, a Flash EEprom system comprises an integrated circuit chip having an array of Flash EEprom cells partitioned into a plurality of sectors, each sector addressable for erase such that all cells therein are erasable simultaneously; characterized by means for selecting a plurality of sectors among the chip for erase operation; and means for simultaneously performing the erase operation on the plurality of selected sectors.

According to a preferred embodiment of the present invention, the Flash EEprom system comprises a plurality of integrated circuit chips each of the type specified above.

According to the present invention, an array of Flash EEprom cells on a chip is organized into sectors such that all cells within each sector are erasable at once. A Flash EEprom memory system comprises one or more Flash EEprom chips under the control of a controller. The invention allows any combination of sectors among the chips to be selected and then erased simultaneously. This is faster and more efficient than prior art schemes where all the sectors must be erased every time or only one sector at a time can be erased. The invention further allows any combination of sectors selected for erase to be deselected and prevented from further erasing during the erase operation. This feature is important for stopping those sectors that are first to be erased correctly to the "erased" state from over erasing, thereby preventing unnecessary stress to the Flash EEprom device. The invention also allows a global de-select of all sectors in the system so that no sectors are selected for erase. This global reset can quickly put the system back to its initial state ready for selecting the next combination of sectors for erase. Another feature of the invention is that the selection is independent of the chip select signal which enables a particular chip for read or write operation. Therefore it is possible to perform an erase operation on some of the Flash EEprom chips while read and write operations may be performed on other chips not involved in the erase operation.

Additional objects, features, and advantages of the present invention will be understood from the following description of its preferred embodiments, which description should be taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

Fig. 1A is a general micrprocessor system including the Flash EEprom memory system of the present invention;

Fig. 1B is schematic block diagram illustrating a system including a number of Flash EEprom memory chips and a controller chip;

Fig. 2 is a schematic illustration of a system of Flash EEprom chips, among which memory sectors are selected to be erased;

Fig. 3A is a block circuit diagram on a Flash EEprom chip for implementing selective multiple sector erase according to the preferred embodiment;

Fig. 3B shows details of a typical register used to

select a sector for erase as shown in Fig. 2A;

Fig. 4 is a flow diagram illustrating the erase sequence of selective multiple sector erase;

Description of the Preferred Embodiments EEprom System

A computer system in which the various aspects of the present invention are incorporated is illustrated generally in Figure 1A. A typical computer system architecture includes a microprocessor 21 connected to a system bus 23, along with random access, main system memory 25, and at least one or more input-output devices 27, such as a keyboard, monitor, modem, and the like. Another main computer system component that is connected to a typical computer system bus 23 is a large amount of long-term, non-volatile memory 29. Typically, such a memory is a disk drive with a capacity of tens of megabytes of data storage. This data is retrieved into the system volatile memory 25 for use in current processing, and can be easily supplemented, changed or altered.

One aspect of the present invention is the substitution of a specific type of semiconductor memory system for the disk drive but without having to sacrifice non-volatility, ease of erasing and rewriting data into the memory, speed of access, low cost and reliability. This is accomplished by employing an array of electrically erasable programmable read only memories (EEprom's) integrated circuit chips. This type of memory has additional advantages of requiring less power to operate, and of being lighter in weight than a hard disk drive magnetic media memory, thereby being especially suited for battery operated portable computers.

The bulk storage memory 29 is constructed of a memory controller 31, connected to the computer system bus 23, and an array 33 of EEprom integrated circuit chips. Data and instructions are communicated from the controller 31 to the EEprom array 33 primarily over a serial data line 35. Similarly, data and status signals are communicated from the EEprom 33 to the controller 31 over serial data lines 37. Other control and status circuits between the controller 31 and the EEprom array 33 are not shown in Figure 1A.

Referring to Figure 1B, the controller 31 is preferably formed primarily on a single integrated circuit chip. It is connected to the system address and data bus 39, part of the system bus 33, as well as being connected to system control lines 41, which include interrupt, read, write and other usual computer system control lines.

The EEprom array 33 includes a number of EEprom integrated circuit chips 43, 45, 47, etc. Each includes a respective chip select and enable line 49, 51 and 53 from interface circuits 40. The interface circuits 40 also act to interface between the serial data lines 35, 37 and a circuit 57. Memory location addresses and data being written into or read from the EEprom chips 43, 45, 47, etc. are communicated from a bus 55, through logic and register circuits 57 and thence by another bus 59 to each of the memory chips 43, 45, 47 etc.

The bulk storage memory 29 of Figures 1A and 1B can be implemented on a single printed circuit card for moderate memory sizes. The various lines of the system buses 39 and 41 of Figure 1B are terminated in connecting pins of such a card for connection with the rest of the computer system through a connector. Also connected to the card and its components are various standard power supply voltages (not shown).

For large amounts of memory, that which is conveniently provided by a single array 33 may not be enough. In such a case, additional EEprom arrays can be connected to the serial data lines 35 and 37 of the controller chip 31, as indicated in Figure 1B. This is preferably all done on a single printed circuit card but if space is not sufficient to do this, then one or more EEprom arrays may be implemented on a second printed circuit card that is physically mounted onto the first and connected to a common controller chip 31.

Erase of Memory Structures

In system designs that store data in files or blocks the data will need to be periodically updated with revised or new information. It may also be desirable to overwrite some no longer needed information, in order to accommodate additional information. In a Flash EEprom memory, the memory cells must first be erased before information is placed in them. That is, a write (or program) operation is always preceded by an erase operation.

In conventional Flash erase memory devices, the erase operation is done in one of several ways. For example, in some devices such as the Intel corporation's model 27F-256 CMOS Flash EEprom, the entire chip is erased at one time. If not all the information in the chip is to be erased, the information must first be temporarily saved, and is usually written into another memory (typically RAM). The information is then restored into the nonvolatile Flash erase memory by programming back into the device. This is very slow and requires extra memory as holding space.

In other devices such as Seeq Technology Incorporated's model 48512 Flash EEprom chip, the memory is divided into blocks (or sectors) that are each separately erasable, but only one at a time. By selecting the desired sector and going through the erase sequence the designated area is erased. While, the need for temporary memory is reduced, erase in various areas of the memory still requires a time consuming sequential approach. See for example, "1-Mbit flash memories seek their role in system design," by Ron Wilson in Computer Design, March 1, 1989,

pp. 30-32.) in which it is described that SEEQ's 1-Mbit memory is further partitioned into 128 individually erasable sectors, each sector being 1 kbyte.

In the present invention, the Flash EEprom memory is divided into sectors where all cells within each sector are erasable together. Each sector can be addressed separately and selected for erase. One important feature is the ability to select any combination of sectors for erase together. This will allow for a much faster system erase than by doing each one independently as in prior art.

Figure 2 illustrates schematically selected multiple sectors for erase. A Flash EEprom system includes one or more Flash EEprom chips such as 201, 203, 205. They are in communication with a controller 31 through lines 209. Typically, the controller 31 is itself in communication with a microprocessor system (not shown). The memory in each Flash EEprom chip is partitioned into sectors where all memory cells within a sector are erasable together. For example, each sector may have 512 byte (i.e. 512x8 cells) available to the user, and a chip may have 1024 sectors. Each sector is individually addressable, and may be selected, such as sectors 211, 213, 215, 217 in a multiple sector erase. As illustrated in figure 2, the selected sectors may be confined to one EEprom chip or be distributed among several chips in a system. The sectors that were selected will all be erased together. This capability will allow the memory and system of the present invention to operate much faster than the prior art architectures.

Figure 3A illustrates a block diagram circuit 220 on a Flash EEprom chip (such as the chip 201 of figure 2) with which one or more sectors such as 211, 213 are selected (or deselected) for erase. Essentially, each sector such as 211, 213 is selected or tagged by setting the state of an erase enable register such as 221, 223 associated with the respective sectors. The selection and subsequent erase operations are performed under the control of the controller 31 (see figure 2). The circuit 220 is in communication with the controller 31 through lines 209. Command information from the controller is captured in the circuit 220 by a command register 225 through a serial interface 227. It is then decoded by a command decoder 229 which outputs various control signals. Similarly, address information is captured by an address register 231 and is decoded by an address decoder 233.

For example, in order to select the sector 211 for erase, the controller sends the address of the sector 211 to the circuit 220. The address is decoded in line 235 and is used in combination with a set erase enable signal in bus 237 to set an output 239 of the register 221 to HIGH. This enables the sector 211 in a subsequent erase operation. Similarly, if the sector 213 is also desired to be erased, its associated register 223 may be set HIGH.

Figure 3B shows the structure of the register such as 221, 223 in more detail. The erase enable register 221 is a SET/RESET latch. Its set input 241 is obtained from the set erase enable signal in bus 237 gated by the address decode in line 235. Similarly, the reset input 243 is obtained from the clear erase enable signal in bus 237 gated by the address decode in line 235. In this way, when the set erase enable signal or the clear erase enable signal is issued to all the sectors, the signal is effective only on the sector that is being addressed.

After all sectors intended for erase have been selected, the controller then issues to the circuit 220, as well as all other chips in the system a global erase command in line 251 along with the high voltage for erasing in line 209. The device will then erase all the sectors that have been selected (i.e. the sectors 211 and 213) at one time. In addition to erasing the desired sectors within a chip, the architecture of the present system permits selection of sectors across various chips for simultaneous erase.

Figures 4(1)-4(11) illustrate the algorithm used in conjunction with the circuit 220 of figure 3A. In figure 4(1), the controller will shift the address into the circuit 220 which is decoded in the line to the erase enable register associated with the sector that is to be erased. In figure 4(2), the controller shifts in a command that is decoded to a set erase enable command which is used to latch the address decode signal onto the erase enable register for the addressed sector. This tags the sector for subsequent erase. In figure 4(3), if more sectors are to be tagged, the operations described relative to figures 4(1)-4(2) are repeated until all sectors intended for erase have been tagged. After all sectors intended for erase have been tagged, the controller initiates an erase cycle as illustrated in figure 4(4).

Optimized erase implementations have been disclosed in U.S. patents 5,095,344, 5,172,338 and 5,163,021. The disclosures of these patents are hereby incorporated by reference. The Flash EEprom cells are erased by applying a pulse of erasing voltage followed by a read to verify if the cells are erased to the "erased" state. If not, further pulsing and verifying are repeated until the cells are verified to be erased. By erasing in this controlled manner, the cells are not subject to over-erasure which tends to age the EEprom device prematurely as well as make the cells harder to program.

As the group of selected sectors is going through the erase cycle, some sectors will reach the "erase" state earlier than others. Another important feature of the present invention is the ability to remove those sectors that have been verified to be erased from the group of selected sectors, thereby preventing them from over-erasing.

Returning to figure 4(4), after all sectors intended for erase have been tagged, the controller initiates an erase cycle to erase the group of tagged sectors. In

figure 4(5), the controller shifts in a global command called Enable Erase into each Flash EEprom chip that is to perform an erase. This is followed in figure 4(5) by the controller raising of the erase voltage line (Ve) to a specified value for a specified duration. The controller will lower this voltage at the end of the erase duration time. In figure 4(6), the controller will then do a read verify sequence on the sectors selected for erase. In figure 4(7), if none of the sectors are verified, the sequences illustrated in figures 4(5)-4(7) are repeated. In figures 4(8) and 3(9), if one or more sectors are verified to be erased, they are taken out of the sequence. Referring also to figure 3A, this is achieved by having the controller address each of the verified sectors and clear the associated erase enable registers back to a LOW with a clear enable command in bus 237. The sequences illustrated in figures 4(5)-4(10) are repeated until all the sectors in the group are verified to be erased in figure 4(11). At the completion of the erase cycle, the controller will shift in a No Operation (NOP) command and the global Enable Erase command will be withdrawn as a protection against a false erasure.

The ability to select which sectors to erase and which ones not to, as well as which ones to stop erasing is advantageous. It will allow sectors that have erased before the slower erased sectors to be removed from the erase sequence so no further stress on the device will occur. This will increase the reliability of the system. Additional advantage is that if a sector is bad or is not used for some reason, that sector can be skipped over with no erase occurring within that sector. For example, if a sector is defective and have shorts in it, it may consume much power. A significant system advantage is gained by the present invention which allows it to be skipped on erase cycles so that it may greatly reduce the power required to erase the chip.

Another consideration in having the ability to pick the sectors to be erased within a device is the power savings to the system. The flexibility in erase configuration of the present invention enables the adaptation of the erase needs to the power capability of the system. This can be done by configuring the systems to be erased differently by software on a fixed basis between different systems. It also will allow the controller to adaptively change the amount of erasing being done by monitoring the voltage level in a system, such as a laptop computer.

An additional performance capability of the system in the present invention is the ability to issue a reset command to a Flash EEprom chip which will clear all erase enable latches and will prevent any further erase cycles from occurring. This is illustrated in figures 3A and 3B by the reset signal in the line 261. By doing this in a global way to all the chips, less time will be taken to reset all the erase enable registers.

An additional performance capability is to have the ability to do erase operations without regard to chip select. Once an erase is started in some of the memory chips, the controller in the system can access other memory chips and do read and write operations on them. In addition, the device(s) doing the erase can be selected and have an address loaded for the next command following the erase.

The various embodiments of the present invention that have been described co-operate in a system of Flash EEprom memory array to make the Flash EEprom memory a viable alternative to conventional non-volatile mass storage devices.

While the embodiments of the present invention that have been described are the preferred implementation, those skilled in the art will understand that variations thereof may also be possible. Therefore, the invention is entitled to protection within the full scope of the appended claims.

Claims

1. A Flash EEprom system (29) comprising:

   an integrated circuit chip (201, 203, 205) having an array of Flash EEprom cells partitioned into a plurality of sectors (211, 213), each sector addressable for erase such that all cells therein are erasable simultaneously;

   characterized by means for selecting (31,220) a plurality of sectors among the chip for erase operation; and

   means for simultaneously performing the erase operation (209, 239) on the plurality of selected sectors.

2. A Flash EEprom system (29) comprising a plurality of integrated circuit chips (201, 203, 205) each of the type specified by Claim 1.

3. A Flash EEprom system (29) as in claim 2, including means adopted for read or write operations on chips which have been enabled by a chip select signal (49, 51, 53), wherein the erase operation is performed on chips without regard to the chip select signal.

4. A Flash EEprom system (29) as in claim 2, wherein the erase operation may be performed on the plurality of sectors selected for erase operation (221, 239), while read, write or other operations may be performed on any other device not selected for erase operation (221, 239).

5. The Flash EEprom system (29) according to claims 1 or 2, further comprising:

   means for individually removing (31, 221, 239) any one or combination of sectors from the plurality of selected sectors, such that said re-

moved sectors are prevented from further erase during the erase operation.

6. The Flash EEprom system (29) according to claims 1 or 2, further comprising:
means for simultaneously deselecting (221, 261) all sectors.

7. The Flash EEprom system (29) according to claims 1 or 2, wherein the selecting means further comprises:
an individual register (221) associated with each sector for holding a status to indicate whether the sector is selected or not.

8. The Flash EEprom system (29) according to claim 7, wherein the simultaneously erasing means is responsive to the status (239) in each of the individual registers (221), such that only the selected sectors are included in the erasing.

9. The Flash EEprom system (29) according to claim 7, wherein any one or combination of the individual registers indicating a selected status are individually resettable (221, 237) to an unselected status.

10. The Flash EEprom system (29) according to claim 7, wherein all the individual registers are simultaneously resettable (221, 261) to a status indicating the associated sectors as not selected.

Patentansprüche

1. Flash-EEPROM-System (29) umfassend:
einen integrierten Schaltkreischip (201, 203, 205) mit einem Feld von Flash-EEPROM-Zellen, die in eine Vielzahl von Sektoren (211, 213) unterteilt sind, wobei jeder Sektor zum Löschen adressierbar ist derart, daß alle in ihm enthaltenen Zellen gleichzeitig löschbar sind,
gekennzeichnet durch Mittel zur Auswahl (31, 220) einer Vielzahl von Sektoren auf dem Chip für eine Löschoperation, und
Mittel zum gleichzeitigen Durchführen der Löschoperation (209, 239) für die Vielzahl ausgewählter Sektoren.

2. Flash-EEPROM-System (29) umfassend eine Vielzahl integrierter Schaltkreischips (201, 203, 205), jedes von der Art wie im Anspruch 1 angegeben.

3. Flash-EEPROM-System (29) nach Anspruch 2, umfassend Mittel, die in der Lage sind, Lese- oder Schreiboperationen an Chips auszuführen, die durch ein Chip-Wählsignal (49, 51, 53) in Bereitschaft versetzt wurden, während die Löschoperation auf Chips ohne Berücksichtigung des Chip-Wählsignals ausgeführt wird.

4. Flash-EEPROM-System (29) nach Anspruch 2, bei dem die Löschoperation für die Vielzahl von zur Löschoperation (221, 239) ausgewählten Sektoren ausgeführt werden kann, während Lese-, Schreib- oder andere Operationen an irgendeiner anderen Vorrichtung, die nicht für die Löschoperation (221, 239) ausgewählt ist, ausgeführt werden können.

5. Flash-EEPROM-System (29) nach Anspruch 1 oder 2 ferner umfassend:
Mittel (31, 221, 239) zur individuellen Entfernung irgendeines oder einer Kombination von Sektoren von der Vielzahl ausgewählter Sektoren derart, daß die entfernten Sektoren vor weiterem Löschen während der Löschoperation geschützt sind.

6. Flash-EEPROM-System (29) nach Anspruch 1 oder 2, ferner umfassend Mittel (221, 261) zur gleichzeitigen Aufhebung des Auswahlzustands aller Sektoren.

7. Flash-EEPROM-System (29) nach Anspruch 1 oder 2, bei dem die Auswählmittel ferner umfassen:
ein jedem Sektor zugeordnetes individuelles Register (221) zum Halten eines Status zur Anzeige, ob der Sektor ausgewählt ist oder nicht.

8. Flash-EEPROM-System (29) nach Anspruch 7, bei dem die gleichzeitig löschenden Mittel auf den Status (239) in jedem der individuellen Register (221) ansprechen derart, daß nur die ausgewählten Sektoren in die Löschung einbezogen werden.

9. Flash-EEPROM-System (29) nach Anspruch 7, bei dem irgendeines oder eine Kombination der individuellen Register, die einen Auswähl-Status anzeigen, einzeln zu einem Nichtauswähl-Status rücksetzbar (221, 237) ist.

10. Flash-EEPROM-System (29) nach Anspruch 7, bei dem alle individuellen Register gleichzeitig zu einem Status rücksetzbar (221, 261) sind, der anzeigt, daß die zugeordneten Sektoren nicht ausgewählt sind.

Revendications

1. Système de Flash EEPROM (29) comprenant :
- un composant de circuit intégré (201,

203, 205) possédant un ensemble de cellules Flash EEPROM divisées en une pluralité de secteurs (211, 213), chaque secteur pouvant être adressé pour un effacement de telle façon que toutes les cellules incluses soient effaçables simultanément;

système caractérisé par un moyen de sélection (31, 220) d'une pluralité de secteurs dans le composant pour une opération d'effacement et par un moyen pour effectuer simultanément l'opération d'effacement (209, 239) sur la pluralité de secteurs choisis.

2. Système de Flash EEPROM (29) comprenant une pluralité de composants de circuit intégré (201, 203, 205), chacun du type spécifié par la revendication 1.

3. Système de Flash EEPROM (29) selon la revendication 2, comprenant un moyen prévu pour des opérations de lecture ou d'écriture sur des composants qui sont validés par un signal de sélection de composant (49, 51, 53), système dans lequel l'opération d'effacement est effectuée sur des composants indépendamment du signal de sélection de composant.

4. Système de Flash EEPROM (29) selon la revendication 2, dans lequel l'opération d'effacement peut être effectuée sur la pluralité de secteurs choisis pour l'opération d'effacement (221, 239) tandis que des opérations de lecture, d'écriture ou d'autres peuvent être effectuées sur un quelconque autre dispositif non choisi pour l'opération d'effacement (221, 239).

5. Système de Flash EEPROM (29) selon la revendication 1 ou 2, comprenant, de plus, un moyen pour l'enlèvement individuel (31, 221, 239) d'un quelconque ou d'une combinaison de secteurs à partir de la pluralité de secteurs choisis de telle façon que lesdits secteurs enlevés ne puissent subir un effacement supplémentaire lors de l'opération d'effacement.

6. Système de Flash EEPROM (29) selon la revendication 1 ou 2, comprenant, de plus, un moyen pour la désélection simultanée (221, 261) de tous les secteurs.

7. Système de Flash EEPROM (29) selon la revendication 1 ou 2, dans lequel le moyen de sélection comprend, de plus, un registre individuel (221) associé à chaque secteur pour la conservation d'un statut indiquant si le secteur est choisi ou non.

8. Système de Flash EEPROM (29) selon la revendication 7, dans lequel le moyen d'effacement simultané est sensible à l'état (239) dans chacun des registres individuels (221) de telle façon que seuls les secteurs choisis soient inclus dans l'effacement.

9. Système de Flash EEPROM (29) selon la revendication 7, dans lequel un quelconque ou une combinaison des registres individuels indiquant un état choisi est réinitialisable de façon individuelle (221, 237) à un état de non sélection.

10. Système de Flash EEPROM (29) selon la revendication 7, dans lequel tous les registres individuels sont réinitialisables simultanément (221, 261) à un état indiquant les secteurs associés comme non sélectionnés.

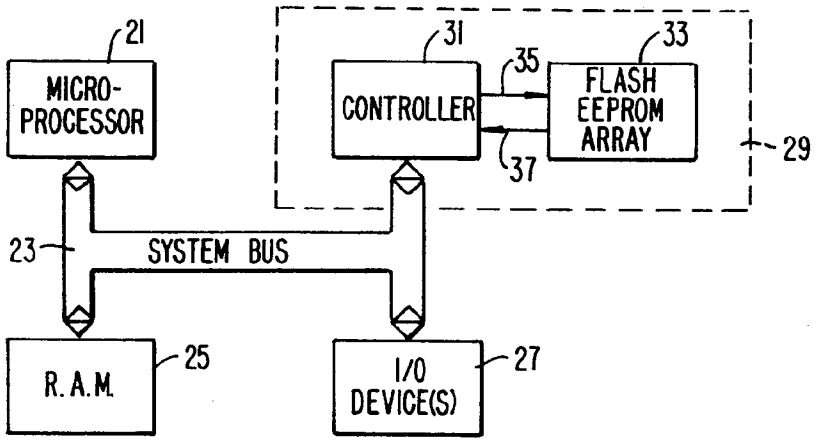
21
MICRO-
PROCESSOR
31
CONTROLLER
35
33
FLASH
EEPROM
ARRAY
37
29
23
SYSTEM BUS
R.A.M.
25
I/O
DEVICE(S)
27

FIG._1A.

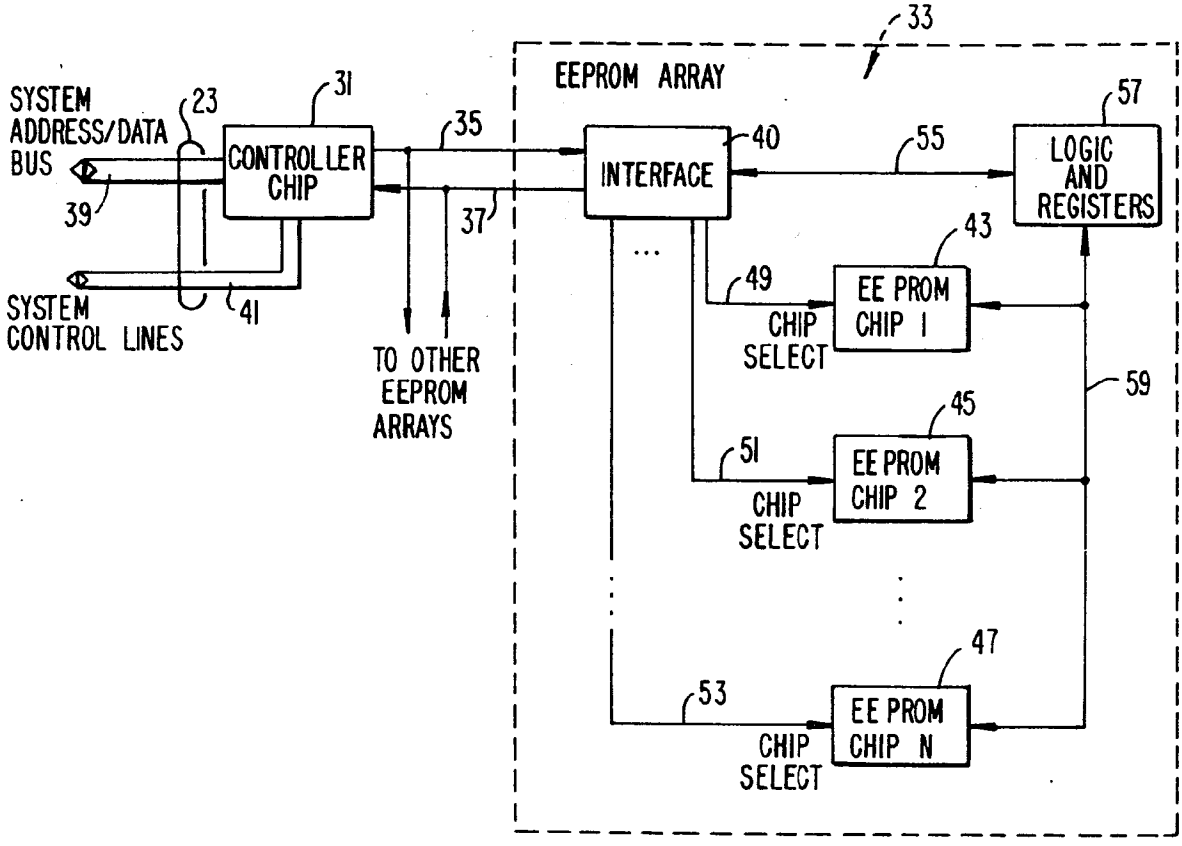
33
EEPROM ARRAY
SYSTEM
ADDRESS/DATA
BUS
23
31
CONTROLLER
CHIP
35
39
37
41
SYSTEM
CONTROL LINES
TO OTHER
EEPROM
ARRAYS
INTERFACE
40
55
57
LOGIC
AND
REGISTERS
43
49
CHIP
SELECT
EE PROM
CHIP 1
59
45
51
CHIP
SELECT
EE PROM
CHIP 2
47
53
CHIP
SELECT
EE PROM
CHIP N

FIG._1B.

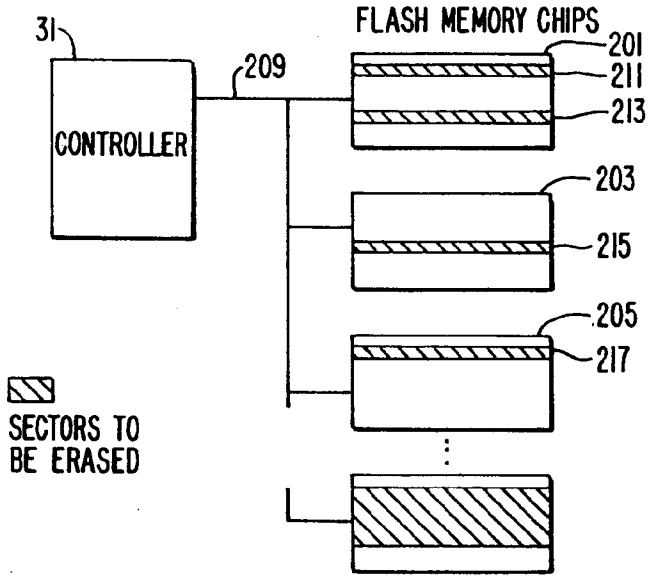

FIG._2.

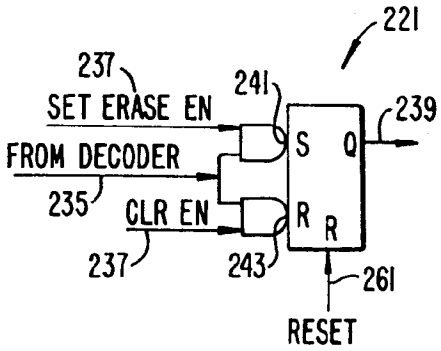

FIG._3B.

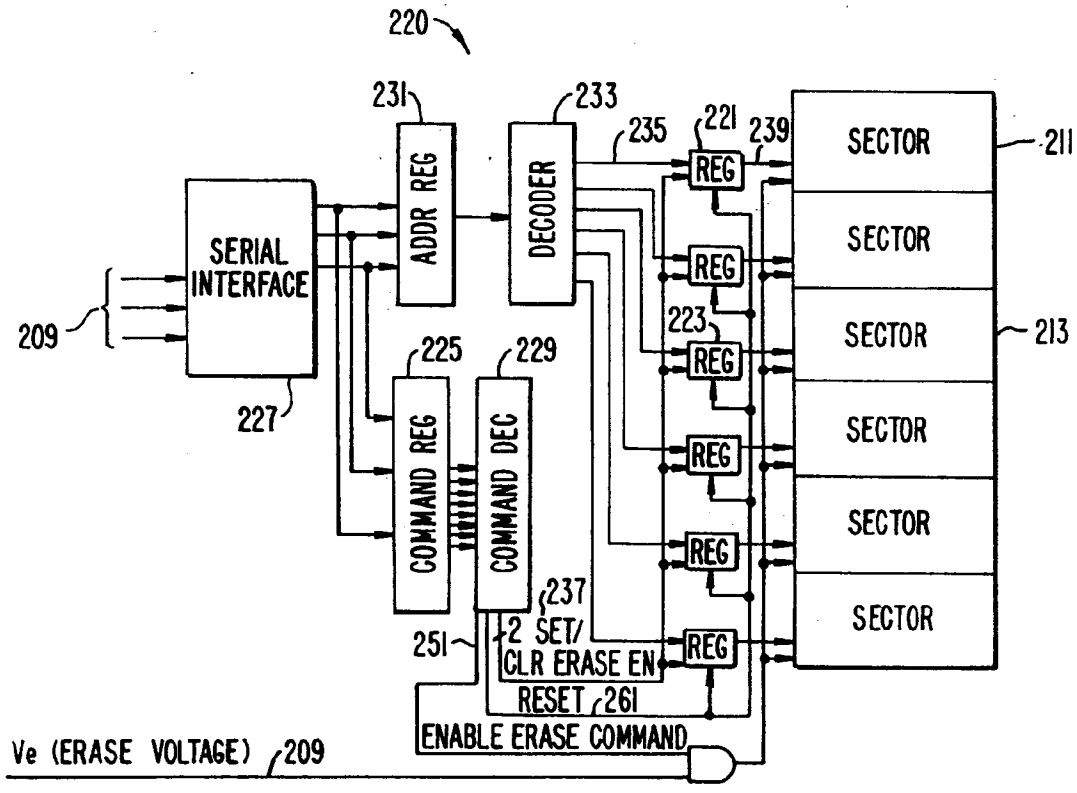

FIG._3A.

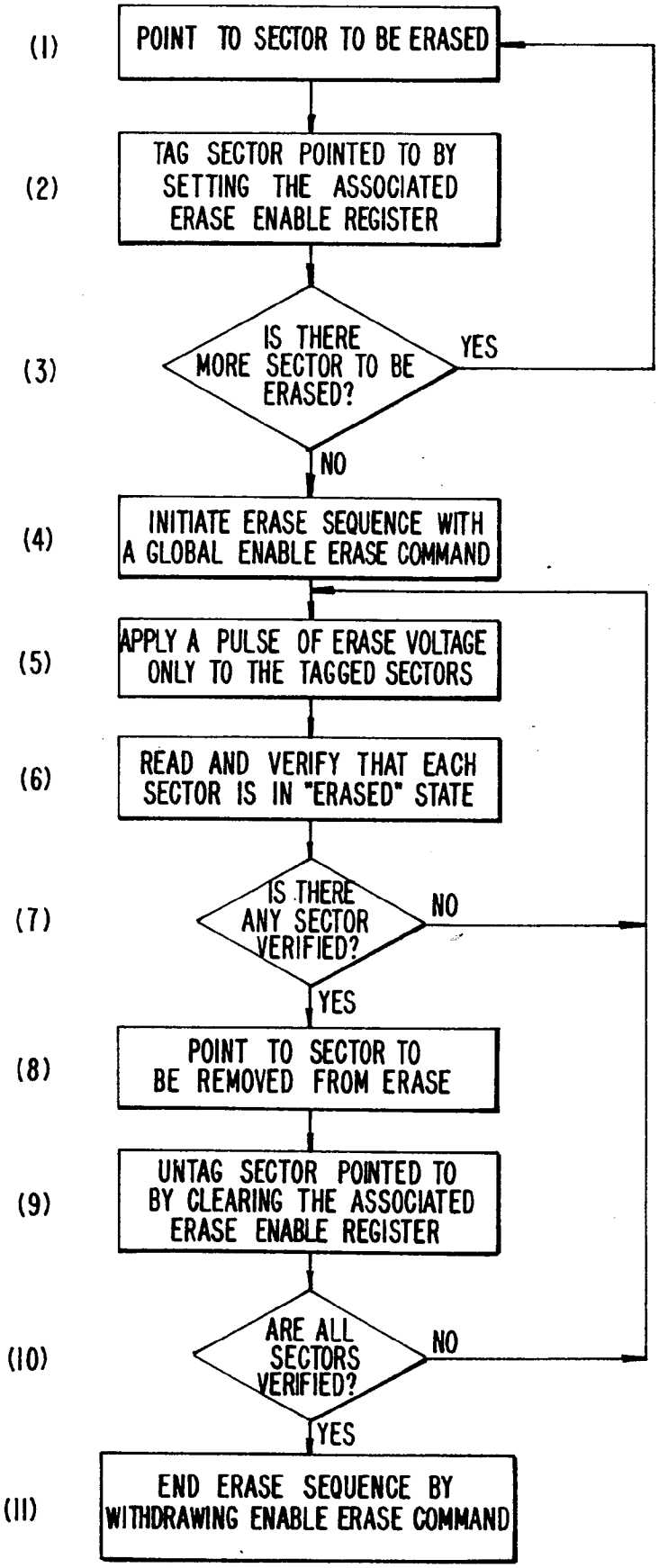
(1)
POINT TO SECTOR TO BE ERASED
(2)
TAG SECTOR POINTED TO BY SETTING THE ASSOCIATED ERASE ENABLE REGISTER
(3)
IS THERE MORE SECTOR TO BE ERASED?
YES
NO
(4)
INITIATE ERASE SEQUENCE WITH A GLOBAL ENABLE ERASE COMMAND
(5)
APPLY A PULSE OF ERASE VOLTAGE ONLY TO THE TAGGED SECTORS
(6)
READ AND VERIFY THAT EACH SECTOR IS IN "ERASED" STATE
(7)
IS THERE ANY SECTOR VERIFIED?
NO
YES
(8)
POINT TO SECTOR TO BE REMOVED FROM ERASE
(9)
UNTAG SECTOR POINTED TO BY CLEARING THE ASSOCIATED ERASE ENABLE REGISTER
(10)
ARE ALL SECTORS VERIFIED?
NO
YES
(11)
END ERASE SEQUENCE BY WITHDRAWING ENABLE ERASE COMMAND

FIG._4.